

## Description

The TKMP2309A uses advanced trench technology and design to provide excellent  $R_{DS(ON)}$  with low gate charge. This device is well suited for use as a load switch or in PWM applications.

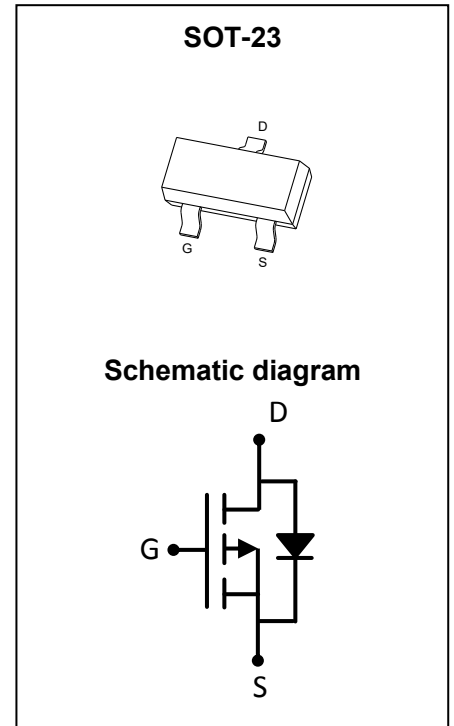
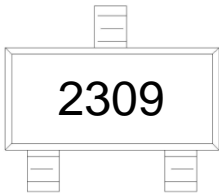
## General Features

- $V_{DS} = -60V, I_D = -4A$   
 $R_{DS(ON)} < 120m\Omega @ V_{GS} = -10V$   
 $R_{DS(ON)} < 170m\Omega @ V_{GS} = -4.5V$
- High density cell design for ultra low  $R_{dson}$
- Fully characterized avalanche voltage and current
- Excellent package for good heat dissipation

## Application

- Load switch
- PWM application

### MARKING:



## Package Marking and Ordering Information

Device	Device Package	Reel Size	Tape width	Quantity
TKMP2309A	SOT-23	Ø180mm	8 mm	3000 units

## Absolute Maximum Ratings ( $T_C = 25^\circ C$ unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	$V_{DS}$	-60	V
Gate-Source Voltage	$V_{GS}$	$\pm 20$	V
Drain Current-Continuous	$I_D$	-4	A
Pulsed Drain Current	$I_{DM}$	-12	A
Maximum Power Dissipation	$P_D$	1.5	W
Operating Junction and Storage Temperature Range	$T_J, T_{STG}$	-55 To 150	$^\circ C$

## Thermal Characteristic

Thermal Resistance, Junction-to-Ambient <sup>(Note 2)</sup>	$R_{\theta JA}$	83.3	$^\circ C/W$
---	-----------------	------	--------------

**Electrical Characteristics ( $T_C=25^\circ\text{C}$  unless otherwise noted)**

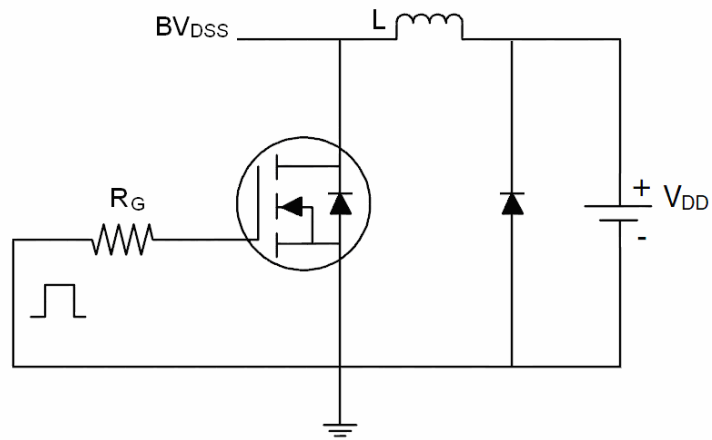
Parameter	Symbol	Condition	Min	Typ	Max	Unit
<b>Off Characteristics</b>						
Drain-Source Breakdown Voltage	$BV_{DSS}$	$V_{GS}=0V, I_D=-250\mu A$	-60	-	-	V
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS}=-60V, V_{GS}=0V$	-	-	-1	$\mu A$
Gate-Body Leakage Current	$I_{GSS}$	$V_{GS}=\pm 20V, V_{DS}=0V$	-	-	$\pm 100$	nA
<b>On Characteristics</b> (Note 3)						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=-250\mu A$	-1.5	-2.2	-3.0	V
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS}=-10V, I_D=-4A$	-	106	120	m $\Omega$
		$V_{GS}=-4.5V, I_D=-3A$	-	135	170	m $\Omega$
Forward Transconductance	$g_{FS}$	$V_{DS}=-5V, I_D=-4A$	-	10	-	S
<b>Dynamic Characteristics</b> (Note 4)						
Input Capacitance	$C_{iss}$	$V_{DS}=-30V, V_{GS}=0V,$ $F=1.0\text{MHz}$	-	930	-	PF
Output Capacitance	$C_{oss}$		-	85	-	PF
Reverse Transfer Capacitance	$C_{rss}$		-	35	-	PF
<b>Switching Characteristics</b> (Note 4)						
Turn-on Delay Time	$t_{d(on)}$	$V_{DD}=-30V, R_L=7.5\Omega,$ $V_{GS}=-10V, R_G=3\Omega$	-	8	-	nS
Turn-on Rise Time	$t_r$		-	4	-	nS
Turn-Off Delay Time	$t_{d(off)}$		-	32	-	nS
Turn-Off Fall Time	$t_f$		-	7	-	nS
Total Gate Charge	$Q_g$	$V_{DS}=-30V, I_D=-4A,$ $V_{GS}=-10V$	-	25	-	nC
Gate-Source Charge	$Q_{gs}$		-	3	-	nC
Gate-Drain Charge	$Q_{gd}$		-	7	-	nC
<b>Drain-Source Diode Characteristics</b>						
Diode Forward Voltage	$V_{SD}$	$V_{GS}=0V, I_S=-4A$	-	-	-1.2	V
Diode Forward Current	$I_S$		-	-	-4	A
Reverse Recovery Time	$t_{rr}$	$T_J = 25^\circ\text{C}, I_F = -4A$	-	25	-	nS
Reverse Recovery Charge	$Q_{rr}$	$di/dt = -100A/\mu s$ (Note 3)	-	31	-	nC

**Notes:**

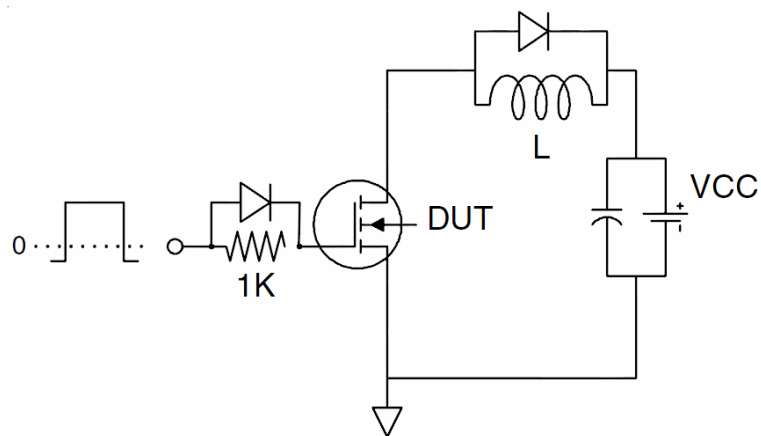
1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board,  $t \leq 10$  sec.
3. Pulse Test: Pulse Width  $\leq 300\mu s$ , Duty Cycle  $\leq 2\%$ .
4. Guaranteed by design, not subject to production

#### Test Circuit

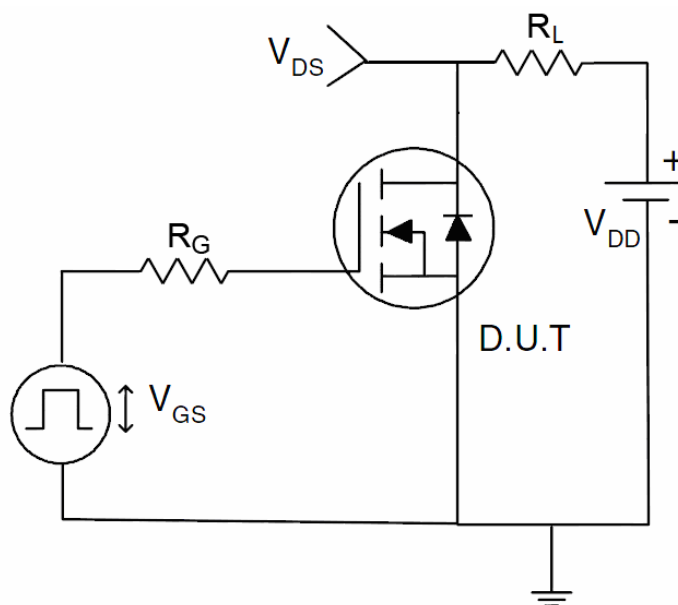
##### 1) E<sub>AS</sub> test Circuit



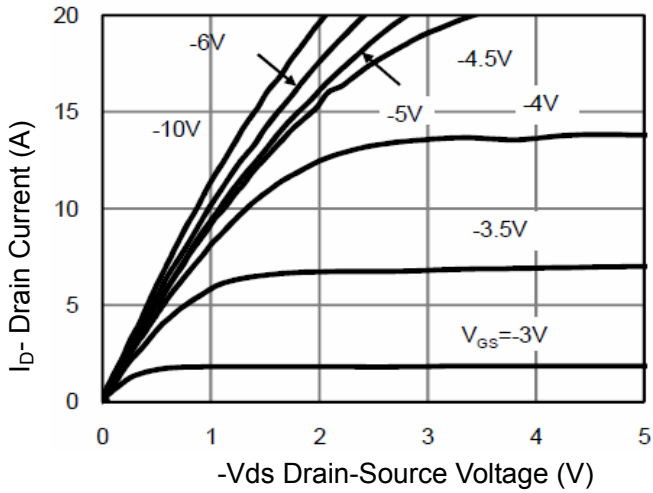
##### 2) Gate charge test Circuit



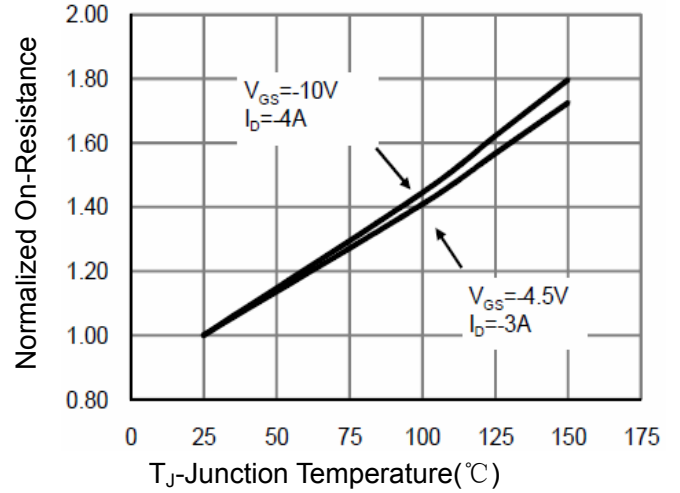
##### 3) Switch Time Test Circuit



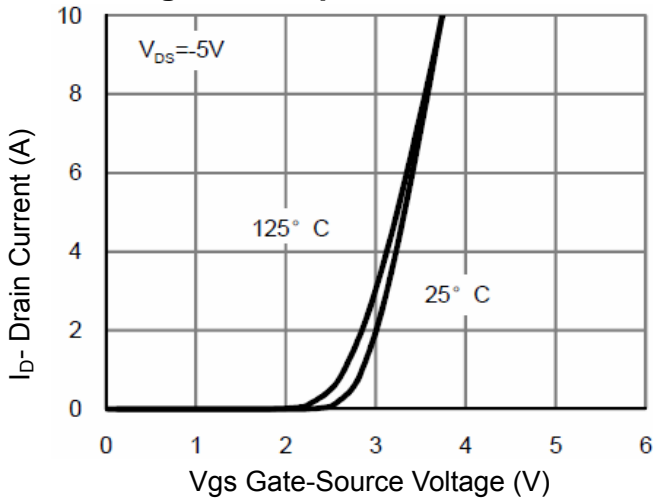
#### Typical Electrical and Thermal Characteristics (Curves)



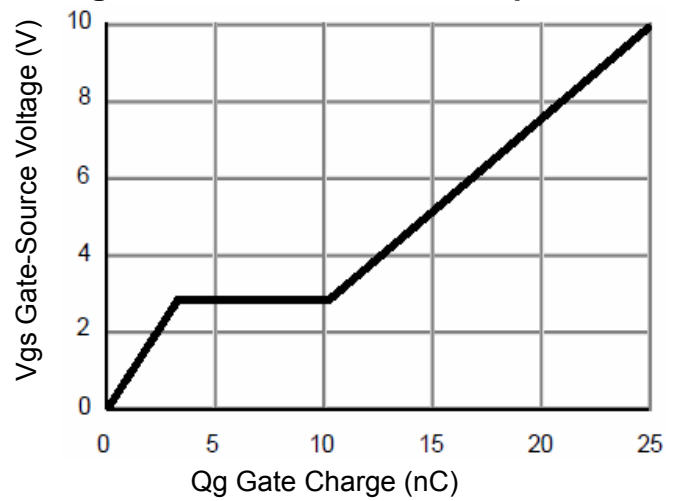
**Figure 1 Output Characteristics**



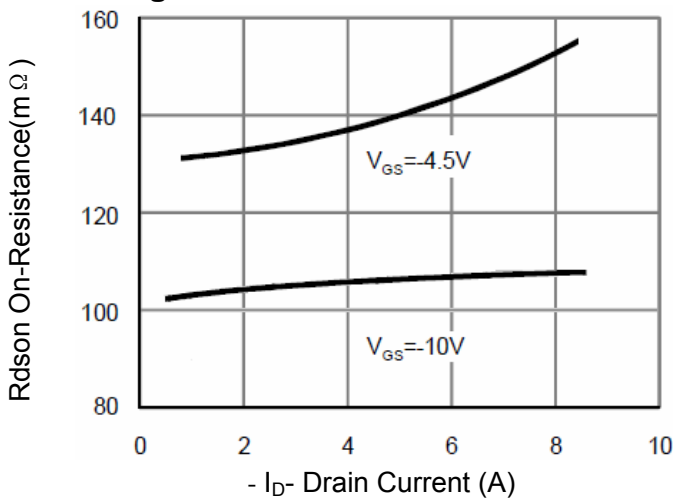
**Figure 4 Rdson-Junction Temperature**



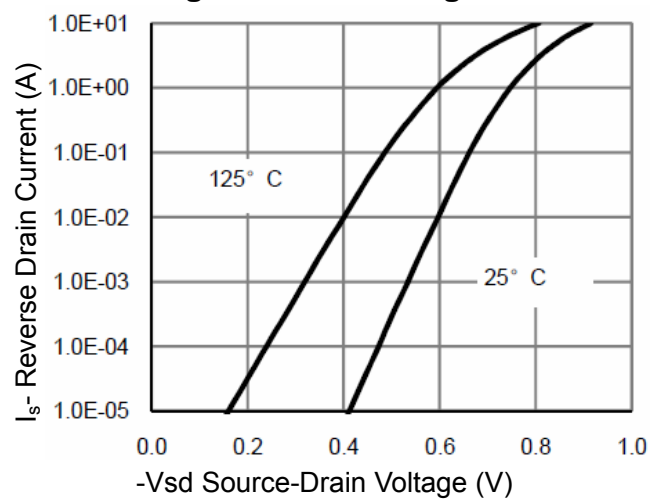
**Figure 2 Transfer Characteristics**



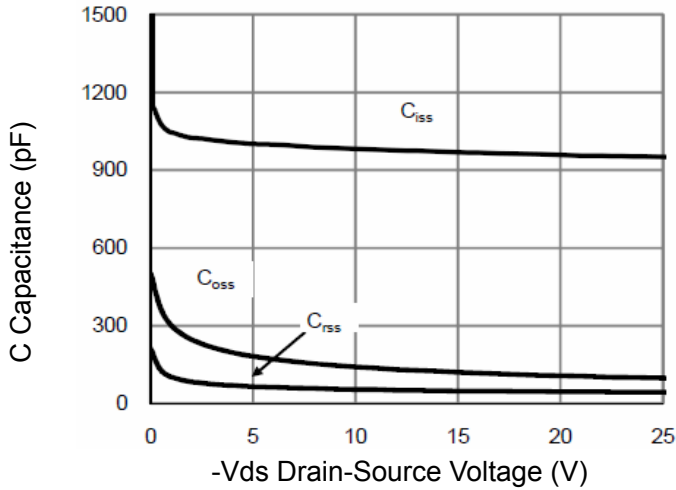
**Figure 5 Gate Charge**



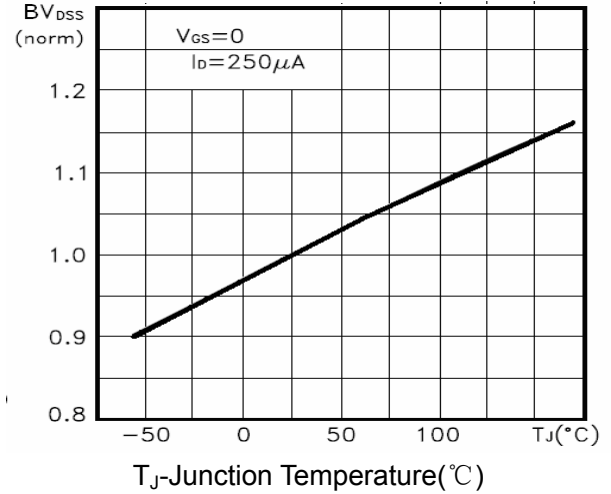
**Figure 3 Rdson- Drain Current**



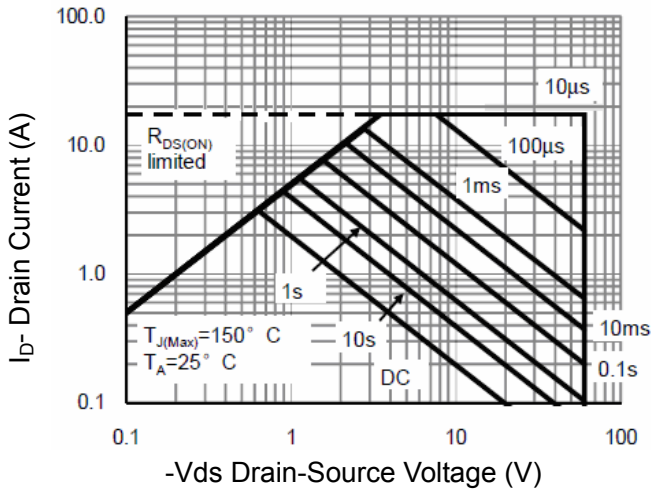
**Figure 6 Source- Drain Diode Forward**



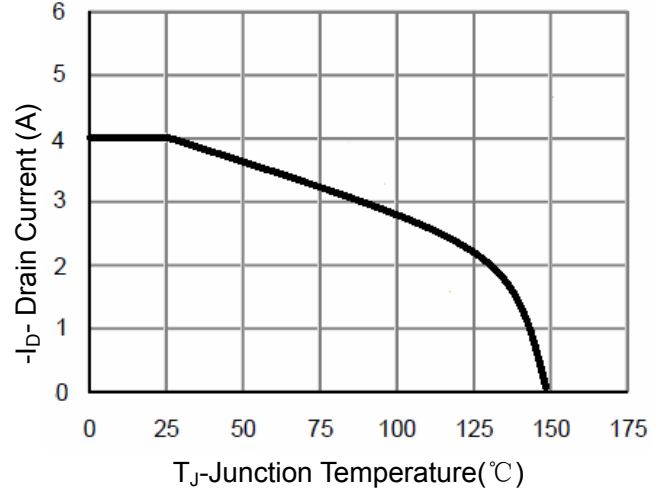
**Figure 7 Capacitance vs Vds**



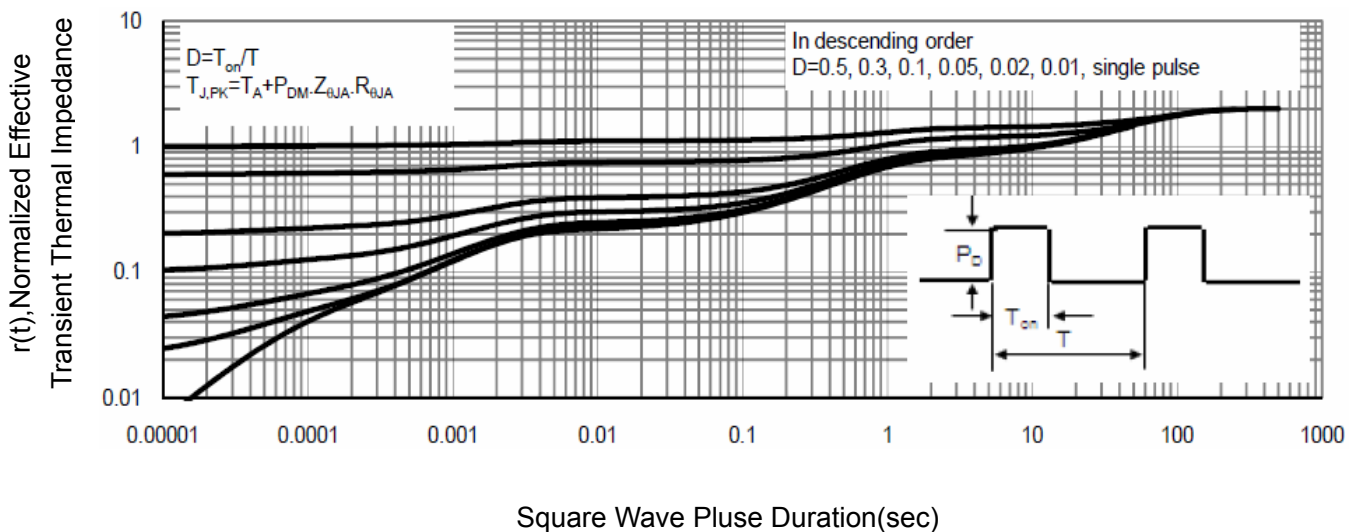
**Figure 9  $BV_{DSS}$  vs Junction Temperature**



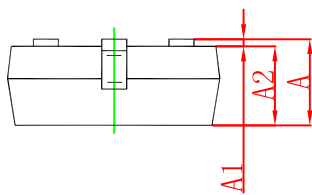
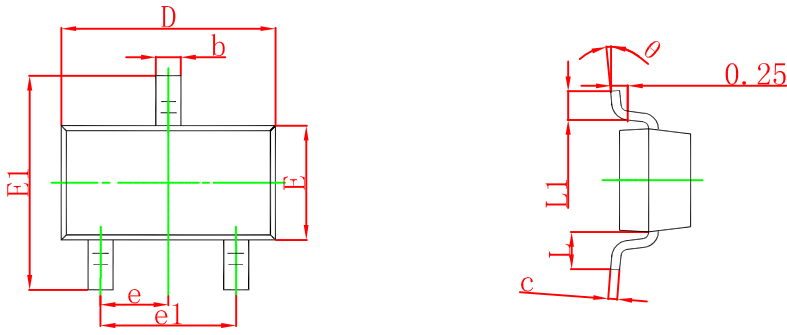
**Figure 8 Safe Operation Area**



**Figure 10  $I_D$  Current De-rating**

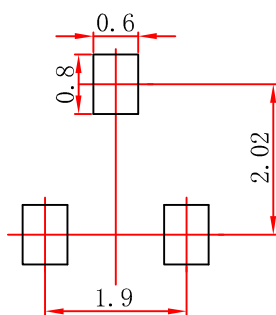


**Figure 11 Normalized Maximum Transient Thermal Impedance**



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.900	1.150	0.035	0.045
A1	0.000	0.100	0.000	0.004
A2	0.900	1.050	0.035	0.041
b	0.300	0.500	0.012	0.020
c	0.080	0.150	0.003	0.006
D	2.800	3.000	0.110	0.118
E	1.200	1.400	0.047	0.055
E1	2.250	2.550	0.089	0.100
e	0.950 TYP		0.037 TYP	
e1	1.800	2.000	0.071	0.079
L	0.550 REF		0.022 REF	
L1	0.300	0.500	0.012	0.020
θ	0°	8°	0°	8°

### SOT-23 Suggested Pad Layout



- Note:
1. Controlling dimension: in millimeters.
  2. General tolerance:  $\pm 0.05$  mm.
  3. The pad layout is for reference purposes only.